Application Data Sheet

Inventor Information

Inventor One Given Name:	Koji
Family Name:	TAKAHASHI
Name Suffix:	
Postal Address Line One	850, Raport Tenri, 2613-1, Ichinomotocho,
Postal Address Line Two	Tenri-shi, Nara 632-0004 Japan
City:	
State or Province:	
Postal or Zip Code:	
Citizenship Country:	JAPAN

Inventor Two Given Name:	Hidenori
Family Name:	KAWANISHI
Name Suffix:	
Postal Address Line One	3-413, Nachuragaden Takanohara, 6-6-1,
Postal Address Line Two	Jingu, Nara-shi, Nara 631-0804 Japan
City:	
State or Province:	
Postal or Zip Code:	
Citizenship Country:	JAPAN

Correspondence Information

Name Line One:	Morrison & Foerster LLP
Name Line Two:	
Address Line One:	755 Page Mill Road
Address Line Two:	
City:	Palo Alto
State or Province:	California
Postal or Zip Code:	94304-1018
Telephone:	(650) 813-5600
Fax:	(650) 494-0792
Electronic Mail:	

Application Information

Title Line One: **METHOD FOR FORMING COMPOUND SEMICONDUCTOR LAYER AND COMPOUND SEMICONDUCTOR APPARATUS**

Title Line Two:	
Total Drawing Sheets:	9
Formal Drawings:	Yes
Application Type:	371 National Phase Application
Docket Number:	299002052200

Representative Information

Representative Customer Number:	25226

Continuity Information

This application is a:	N/A
> Application One:	
Filing Date:	
which is a:	
>>Application Two:	
Filing Date:	
which is a:	
>>>Application Three:	
Filing Date:	

Prior Foreign Applications

Foreign Application One:	10-259015
Filing Date:	September 11, 1998
Country:	JAPAN
Priority Claimed:	Yes
Foreign Application Two:	PCT/JP99/01952
Filing Date:	April 12, 1999
Country:	PCT
Priority Claimed:	Yes